WHAT IS CLAIMED IS:

1. A bandgap reference circuit comprising:

first, second and third current sources CS1, CS2, and CS3 adjusted to have the same current, the first current source feeding into a first BJT device module Q1, the second current source feeding into a second BJT device module Q2 through a first resistor R1, and the third current source connecting to a grounding voltage supply through a second resistor R2;

a current summing circuit;

a first voltage passing unit connecting an output of CS1 as its input and connecting its output to a first end of a third resistor R3 and a first output of the current summing circuit;

a second voltage passing unit connecting an output of CS3 as its input and feeding its output to a first end of a fourth resistor R4 and a second output of the current summing circuit;

a fifth resistor R5 connecting to a third output of the current summing circuit on a first end and the grounding voltage supply on a second end thereof,

wherein a first current through R5 bears a substantially linear relationship with a summation of a second current through R3 and a third current through R4,

wherein the outputs of the first and second voltage passing units track their respective inputs, and

wherein by selecting predetermined values for R1, R2, R3, R4, and R5 in conjunction with selections of Q1 and Q2, a reference voltage of the circuit across R5 is independent of temperature variations.

2. The circuit of claim 1 further comprises an operational amplifier with its negative input connected to the output of CS1 and positive input connected with the

output of CS2.

3. The circuit of claim 1 wherein the current summing circuit provides the first current through R5 equal to the summation of the second and third currents through R3 and R4.

4. The circuit of claim 1 wherein Q2 has a predetermined number of BJT transistors connected in parallel.

5. The circuit of claim 1 wherein the reference voltage is less than or equal to about 1V.

6. The circuit of claim 1 wherein a supply voltage of the circuit is less than about 1V.

7. The circuit of claim 1 wherein Q1 is a pnp type and receives the output of CS1 at its emitter, and wherein Q2 is a pnp type and receives the output of CS2 at its emitter through R1.

8. The circuit of claim 7 wherein a predetermined relationship among an emitter voltage of Q1 (V_{be1}) and an emitter voltage of Q2 (V_{be2}) and the resistors (R5 / R3) * dV_{be1}/dT + ((R2 * R5) /(R1 * R4)) * $d(V_{be1} - V_{be2})/dT$ is zero, wherein dV_{be1}/dT and $d(V_{be1} - V_{be2})/dT$ are respective changes of the emitter voltage of Q1 and a difference between the emitter voltages of Q1 and Q2 with respect to temperature.

9. The circuit of claim 1 wherein Q1 and Q2 have their collectors grounded so that the reference voltage (V_{REF}), an emitter voltage of Q1 (V_{be1}), an emitter voltage

of Q2 (V_{be2}), and the resistors bear a predetermined relationship as represented mathematically by $V_{REF} = V_{be1} * (R5 / R3) + (V_{be1} - V_{be2}) * ((R2 * R5) / (R1 * R4))$.

10. The circuit of claim 1 wherein the first and second voltage passing units are unit gain buffers.

11. A bandgap reference circuit comprising:

first, second and third current sources CS1, CS2, and CS3 with an output of CS1 output feeding into a first BJT device module Q1, an output of CS2 feeding into a second BJT device module Q2 through a first resister R1, and an output of CS3 connecting to a grounding voltage supply through a second resister R2;

a current summing circuit for providing three current paths to the grounding voltage supply through three resistors R3, R4, and R5 respectively,

wherein the outputs of CS1 and CS3 are buffered and connected to the grounding voltage supply through R3 and R4 respectively,

wherein a temperature independent reference voltage (V_{REF}) across R5 is generated when an emitter voltage of Q1 (V_{be1}), an emitter voltage of Q2 (V_{be2}), and the resistors bear a predetermined relationship as represented mathematically by $(R5 / R3) * dV_{be1}/dT + ((R2 * R5) / (R1 * R4)) * d(V_{be1} - V_{be2})/dT = 0$, wherein dV_{be1}/dT and $d(V_{be1} - V_{be2})/dT$ are respective changes of the emitter voltage of Q1 and a difference between the emitter voltages of Q1 and Q2 with respect to temperature.

12. The circuit of claim 11 further comprises an operational amplifier with its negative input connected to the output of CS1 and positive input connected with the output of CS2.

13. The circuit of claim 11 wherein the current summing circuit provides the

current through R5 to be proportional to the summation of the currents through R3 and R4.

14. The circuit of claim 11 wherein Q2 has a predetermined number of BJT transistors similar to Q1 connected in parallel.

15. The circuit of claim 1 wherein the reference voltage is less than or equal to about 1V.

16. The circuit of claim 1 wherein a supply voltage of the circuit is less than about 1V.

17. The circuit of claim 1 wherein Q1 is a pnp type and receives the output of CS1 at its emitter, and wherein Q2 is a pnp type and receives the output of CS2 at its emitter through R1.

18. The circuit of claim 1 further comprises first and second unit gain buffers setting voltages across R3 and R4 by passing the outputs of CS1 and CS3.

19. A method for generating a temperature independent reference voltage, the method comprising:

generating first, second and third current outputs CS1, CS2, and CS3, with CS1 feeding into an emitter of a first pnp BJT device module Q1, CS2 feeding into an emitter of a second pnp BJT device module Q2 through a first resister R1, and CS3 connecting to a grounding voltage supply through a second resister R2;

providing three current paths from a current summing circuit to the ground voltage supply through three resistors R3, R4, and R5 respectively;

imposing an emitter voltage of Q1 (V_{be1}) across R3;

imposing a voltage across R2 to be across R4,

wherein a temperature independent reference voltage (V_{REF}) across R5 is generated when V_{be1}, an emitter voltage of Q2 (V_{be2}), and the resistors bear a predetermined relationship as represented mathematically by (R5 / R3) * dV_{be1}/dT + ((R2 * R5) /(R1 * R4)) * $d(V_{be1} - V_{be2})/dT$ =0, wherein dV_{be1}/dT and $d(V_{be1} - V_{be2})/dT$ are respective changes of the emitter voltage of Q1 and a difference between the emitter voltages of Q1 and Q2 with respect to temperature.

20. The circuit of claim 19 further comprises using an operational amplifier with its negative input connected to CS1 and positive input connected with CS2 for maintaining a same current through Q1 and Q2.

21. The circuit of claim 19 wherein the current summing circuit provides the current through R5 to be proportional to the summation of the currents through R3 and R4.

22. The circuit of claim 19 wherein the reference voltage is less than or equal to about 1V.